STP1090A/STP1091 Multi-Cache Controller Addendum

For use with
SuperSPARC and Multi-Cache Controller
User's Manual

SPARC *Technology Business*

Sun

A Sun Microsystems, Inc Business
2550 Garcia Avenue, Mountain, View, CA U S A. 94043
(408) 774-8545

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2550 Garcia Avenue, Mountain View, California 94043-1100 U.S.A

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Multi-Cache Controller Addendum B

This document details Multi-Cache Controller (MXCC) implementation changes between the different revisions. It is meant to be a guide to implementors and users and should be used as an addendum to the document *SuperSPARC and Multi-Cache Controller User's Manual*, available from STB. For a description of SuperSPARC-to-SuperSPARC II changes, please refer to the document *SuperSPARC II Addendum*, also available from STB All references to SuperSPARC in this *Multi-Cache Controller Addendum* document also apply to SuperSPARC II.

The Multi-Cache Controller chip (MXCC) controls the external 2nd-level cache (E-Cache) of a SuperSPARC processor module and provides the interface for SuperSPARC to connect to the rest of the system. MXCC is designed to support both MBus-based system and XBus/XDBus-based system which have an external cache and use SuperSPARC as the processor chip.

The E-Cache is organized as a direct-map cache Its size can be 1MB or optionally 2MB (for XBus-based system only) and 1/2 MB (for MBus-based systems). Eight 128Kx9 (or 128Kx8) pipelined SRAM chips are used for the 1MB configuration

Shaded entries in tables indicate MXCC implementation changes pertinent to that revision.

B.1 External Cache Support

The MXCC chip can completely implement a large, directly mapped, physically addressed external cache The MXCC serves as a single-chip interface to the level-2 MBus standard and as multiprocessor (a general-purpose packet-switched interface for the XBus) to a variety of bus standards.

Both SuperSPAR and the MXCC are optimized to work with fully pipelined cache RAMs, and they both support SPARC's total store ordering (TSO) and partial store ordering (PSO) memory models See the *SPARC Architecture Manual* and Memory Model for more details.

B.2 Multiprocessor Cache Coherence Support

SuperSPARC provides built-in multiprocessor cache coherence. The protocol supports multiple-cached copies of shared data.

Bus snooping implements the coherence algorithms. All coherence protocols are based on physical addresses.

B.3 MXCC 1090 - 1090A Changes

The following are the changes put into STP1090A.

B.3.1 Architectural changes for bug fixes, performance and speed

A new Multi Command (MC) Mode for XBus Systems was added. The original MC behavior is accessible by setting a new bit in the control register.

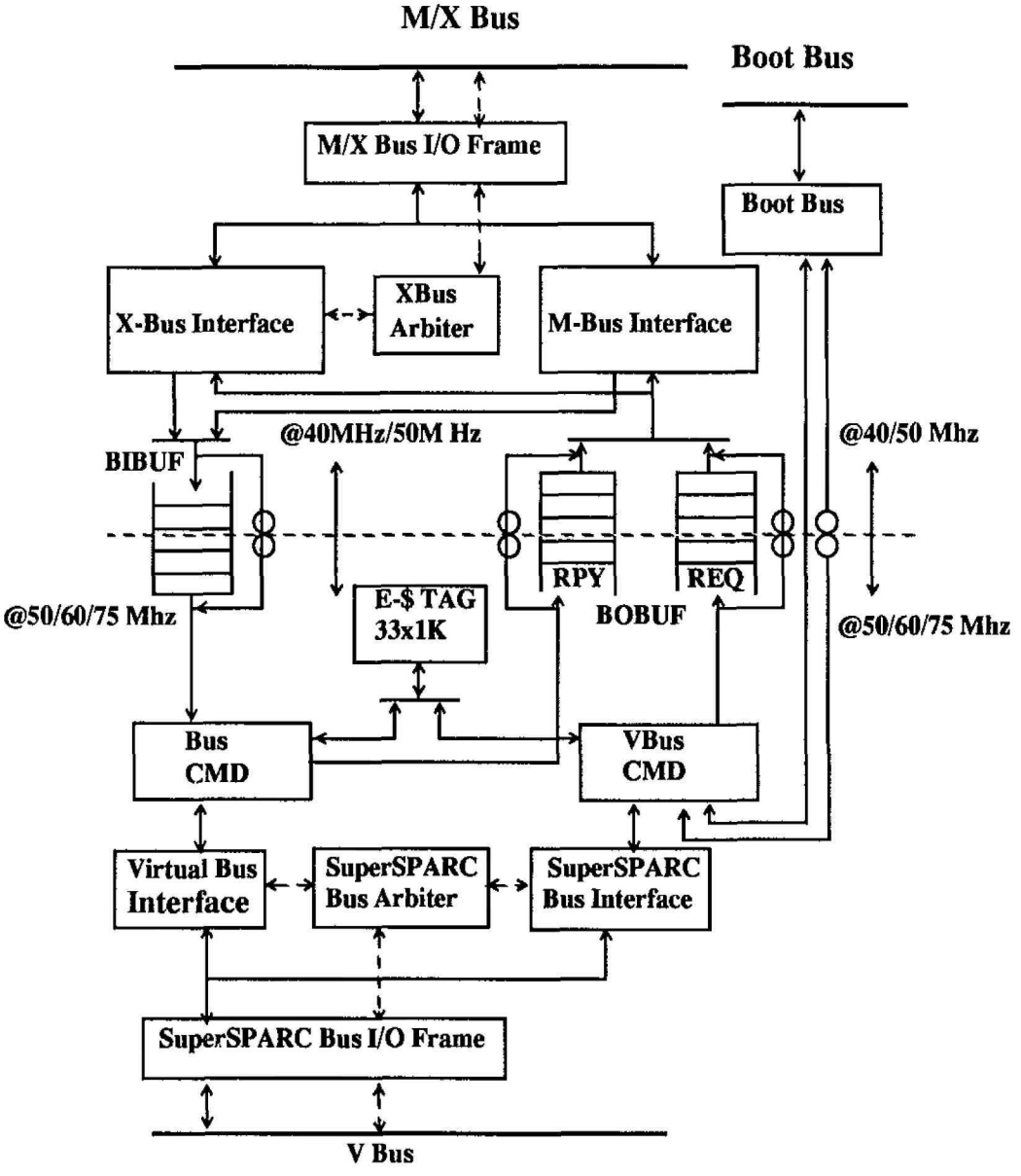
Table B-1 MXCC Control Register

Rsvd			DBC		WI	PF	MC	PE	CE	CS	HC
31	9	8		7	6	5	4	3	2	1	0

MC: Multiple Command Enable. When this bit is set to one, MXCC is allowed to issue multiple commands without waiting for their completion

Note – No change in Multi Command support for MBus Systems.

MXCC Functional Block Diagram



B.3 2 Fixed Coherent Invalidates on first Write feature in MXCC

First writes to clean non shared lines used to take 17 cycles but is now completed in 5 cycles This enhancement is useful in MBus systems where earlier, first writes were done by sending out a false CI on the bus and on completion of the CI, the store would be acknowledged

B.3 3 Modified PEND_ protocol for Non-Cacheable Stores

In MBus systems the average non-Cacheable store latency was in the order of 17 cycles, but is now 6 cycles This enhancement also helps XBus based systems where non-Cacheable store latency is greatly reduced. Prior to this change, non-cacheable stores were dealt with like regular cacheable stores, by the assertion of PEND_ which guaranteed TSO. The current implementation now allows for the CPU's store buffer to stream out back-to-back non-cacheable stores as MXCC no longer asserts PEND_. With any other kind of store, MXCC retries it asserts PEND_. This ensures that the outstanding non-cacheable stores complete before PEND_ is deasserted allowing for any other store. MXCC continues to assert PEND_ for Cacheable stores.

B.3.4 Improved Write Back Performance

Improved Write Back performance when 1, 2 or 3 sub blocks are to be flushed. This is done by looking at all the status bits of a cache line at the same time. This enhancement helps both XBus and MBus based systems. The improvement in writeback is a function of the state of the sub-blocks, and thus varies. The advantage of faster completion of writebacks is that outstanding load/store misses can get processed faster without being blocked by a writeback in progress. This has been a major bottleneck in MXCC performance and this change alleviates the problem to some extent.

B 3.5 Improved Internal Arbitration mechanism for VBus

This helps reduce snoop data latency in MBus systems from A+18 to A+12. It also helps all systems in latencies for loads, prefetches by an order of 1-2 cycles on the average The changes were done based on determining inherent inefficiencies in internal bus arbitration policies.

B.3 6 ADDR20_ pin for 2 MB E-Cache Support

Added ADDR20_ pin for 2 MB ECache support for XBus based systems

B.4 MXCC STP1090A-H33xxxxxx Changes

The following are the changes put into STP1090A with mask revision H33xxxxxx

B.4.1 Failure to set Shared Bit on Owned Cache Tag Lines (XBus Mode only) Bug Fix

In an XBus system, the shared bit is not being set for a foreign GetBlock. This is seen under a heavy XBUS load and with multiple processors (7 or greater). The inbound queue BIBUF gets backed up and the TCMD field in the datacycle of the GetBlock gets corrupted.

B 4.2 IO Drivers:

IO Driver enables optimized to meet greater than 75Mhz timing

B.5 MXCC STP1090A - STP1091 Changes

The following are the changes put into STP1091.

B 5.1 1/2 MB External Cache support for MBus based systems

Control register configuration to select cache size.

B.5.2 New IO Cells optimized to meet greater than 90 Mhz

B.5.3 Increased MTBF for Synchronizers

Mean Time Before Failure for clock synchronizers increased for higher frequencies.

B.5.4 New Pinout & Package (7 new pins)

Package

New package due to change in die size, bond compaction, chip capacitors on package and increased number of power and ground pins.

4 PMC Pins

Process monitor control pins for manufacturing use only.

2 Thermal Diode Pins

Thermal diode pins to aid in temperature measurements.

ADDR20_

Address <20>_ for 2 MByte address select. This pin eliminates an additional discrete component on the SuperSPARC module

B.6 MXCC Revisions

Table B-2 MXCC Versions - JTAG CID and MBus Port

Control Register	JTAG.CID	MPORT.MREV
Revision	32 Bits	4 Bits
1 X	0000302F	0
2 0	4000302F	4
2.X	5000302F	4
3 1	9000302F	9
3 3	A000302F	9
4 0	C000302F	c

Table B-3 External Cache Configuration XBus Based Systems

E-Cache Size	CS	HC
1 MB	0	0
1/2 MB	0	1
2 MB	1	0
1 MB	1	1

Table B-4 External Cache Configuration - MBus Based Systems

E-Cache Size	CS	HC
1MB	0	0
1/2 MB	0	1
1 MB	1	0
1 MB	1	1

CS : Cache Size

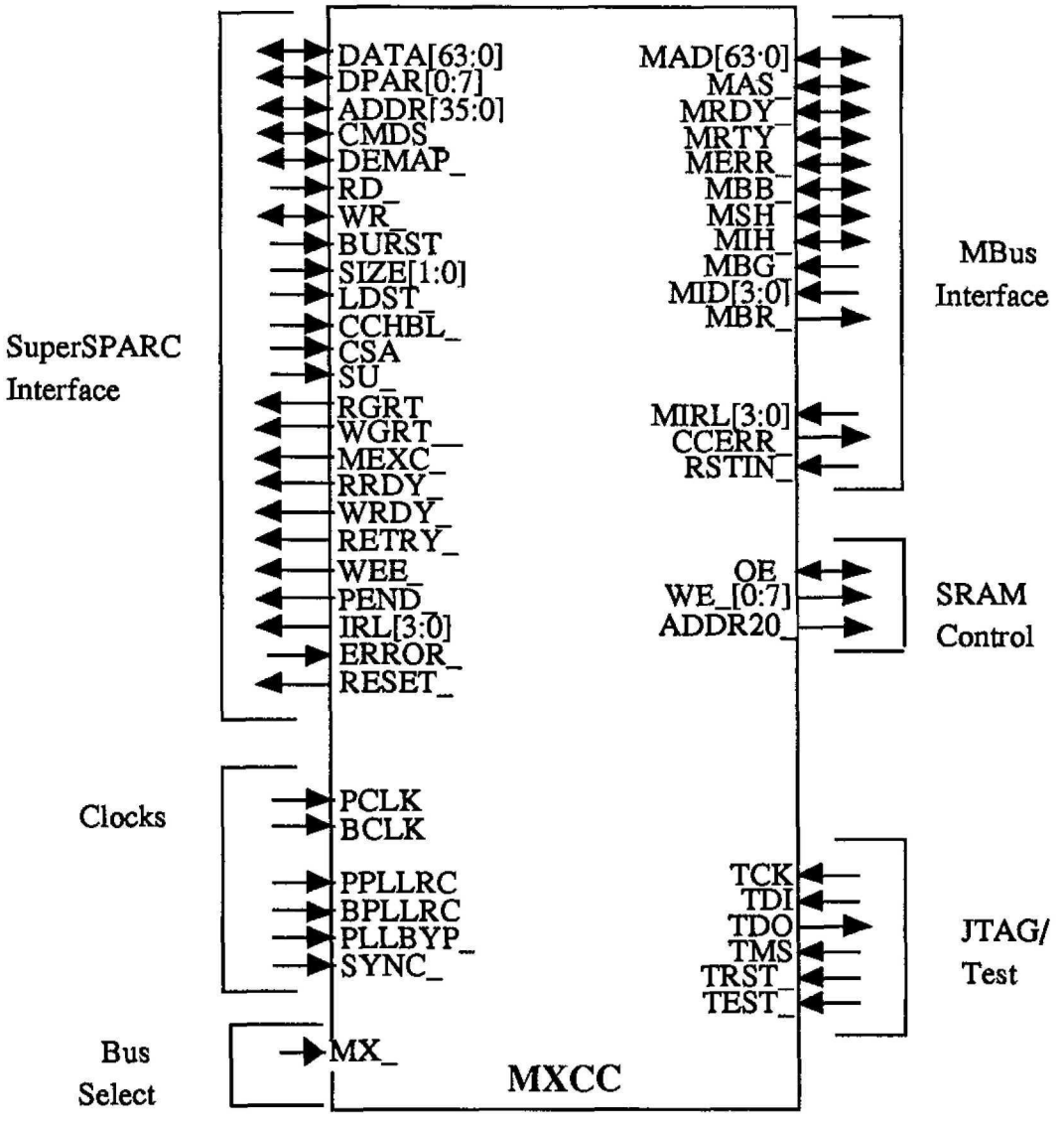
HC: Half Cache

1090A is 3 X and 1091 is 4 X

B.7 MXCC 4.X - STP1091 Statistics

Table B-5 MXCC 1091 Chip Statistics

Description	
Target Cycle Time	90 Mhz
Die Size	12 9 x 12 9 mm
Est Power Consumption	6 0 W
Power Supply	4 8 V
Process	0 6u GS2
Transistor Count	2 277 M
Pin out	258 Active Pads 191 VCC/VSS 1 SPARE



Total Signal I/O: 238

Figure B-1. MXCC in MBus Configuration

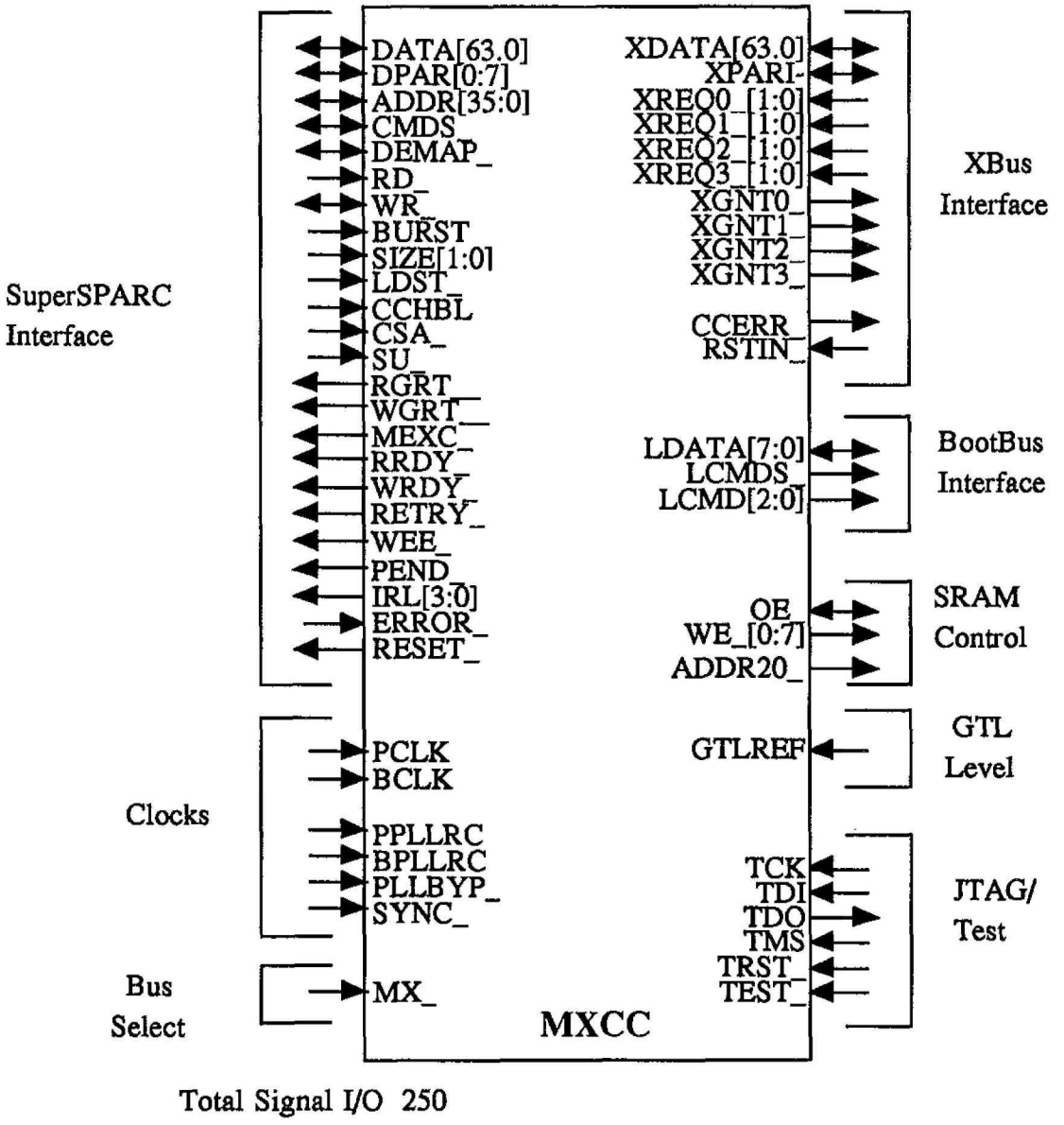
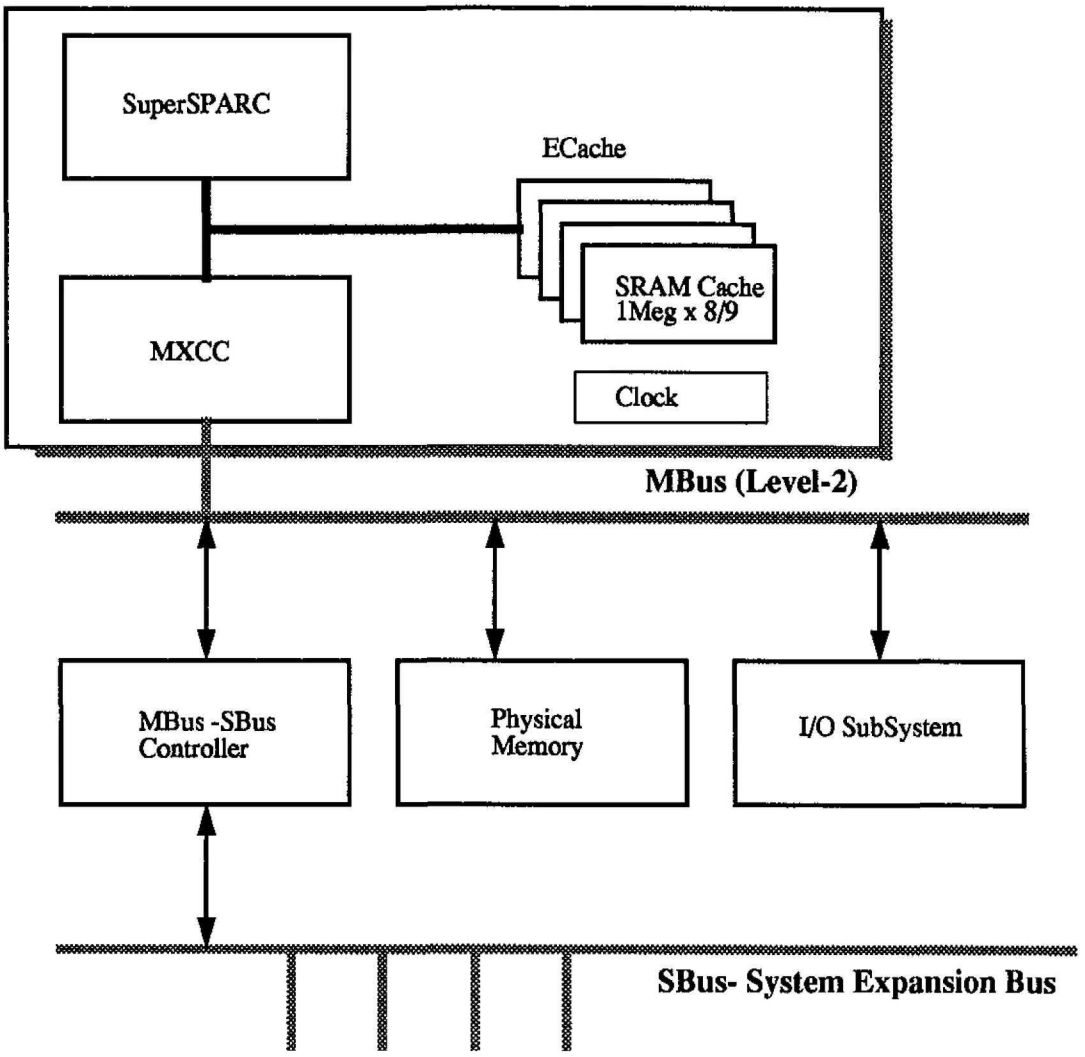


Figure B-2. MXCC in XBus Configuration

MXCC MBus Based Module Interface



MXCC XBus Based Module Interface